

Coarse Grain Reconfigurable Architectures Polymorphism In Silicon Cores

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Coarse Grain Reconfigurable Architectures Polymorphism

coarse grain reconfigurable arrays (RAs) with pathwidths greater The KressArray is primarily a mesh of rDPUs physically connected through wiring by abutment: no extra routing areas needed.. In 1995 it has been flexibility micro- processor Fig. 2: Bridg-ing the gap. than 1 bit, because fine-grained architectures are much less

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Coarse-Grained Reconfigurable Architectures ... This approach to polymorphism provides better performance across a wide range of application types than an approach in which many small ...

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Example of a Coarse-Grained Reconfigurable Architecture. We propose a modulo scheduling technique for CGRA architectures that leverages graph embedding commonly used in graph layout and visualization, referred to as modulo graph embedding.

CCCP: Coarse-Grained Reconfigurable Architecture

INTRODUCTION : #1 Coarse Grain Reconfigurable Architectures Polymorphism Publish By Debbie Macomber, Coarse Grain Reconfigurable Architectures coarse grained architectures provide operator level cfbs word level datapaths published as rdpareconfigu able datapath array kress has been coined later the kressarray is a super systolic array ...

coarse grain reconfigurable architectures polymorphism in ...

coarse grain reconfigurable arrays (RAs) with pathwidths greater than 1 bit, because fine-grained architectures are much less efficient because of a huge routing area overhead and poor routability [2]. Since computational datapaths have regular structure, full custom designs ofreconfigurable datapath units

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of this coarse grain reconfigurable architectures polymorphism in silicon cores can be taken as capably as picked to act. You can also browse Amazon's limited-time free Kindle books to find out what books are free right now. You can sort this list by the average customer review rating as well as by the book's publication date.

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From Physical Implementation

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Reconfigurable architectures have gained popularity in recent years as they allow the design of energy-efficient accelerators. Fine-grain fabrics (e.g. FPGAs) have traditionally suffered from performance and power inefficiencies due to bit-level reconfigurable abstractions. Both fine-grain and coarse-grain architectures (e.g. CGRAs) tradi-

Plasticine: A Reconfigurable Architecture For Parallel ...

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To partially address this, a polymorphic approximate coarse-grained reconfigurable architecture (PX-CGRA), which contains precision-scalable processing elements (PEs), is introduced in [21].

PX-CGRA: Polymorphic approximate coarse-grained ...

Coarse Grain Reconfigurable Architectures, a Survey

(PDF) Coarse Grain Reconfigurable Architectures, a Survey ...

Abstract: This paper presents a methodology for designing an approximate coarse-grained reconfigurable architecture (X-CGRA), and its use for accelerating both error-resilient and error-sensitive applications. The output quality of the X-CGRA is manageable at the run-time for better performance and power/energy consumption tradeoffs.

Toward Approximate Computing for Coarse-Grained ...

Coarse-grained reconfigurable architectures in the past 25 years: Overview and classification. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS'16). 235--244. Google Scholar; H. Amano. 2006. A survey on dynamically reconfigurable processors.

A Survey of Coarse-Grained Reconfigurable Architecture and ...

Abstract: In this contribution we apply a novel strategy for partial remapping to significantly enhance the reliability of coarse-grained reconfigurable architectures. If a component of the architecture is affected by a permanent error, it will be deactivated and the architecture is reconfigured to relinquish the concerned resource.

Spatial and Temporal Data Path Remapping for Fault ...

(a) Island style coarse-grained spa-tial computer (b) Pipelined coarse-grained reconfigurable array Figure 2. CGRA Block Diagrams 2. Exploring Coarse-grained Architectures To create a CGRA that is focused on datapath com-putations for a particular application domain is a bal-ancing act akin to designing an ASIC and a FPGA si-multaneously.

Designing a Coarse-grained Reconfigurable Architecture for ...

Coarse-grain reconfigurable architectures. Flexibility inlining. Canonical interconnection. Carry-save arithmetic. Chain addition. Array multiplier. Recommended articles Citing articles (0) Sotirios Xydis received his Diploma in Electrical and Computer Engineering from the National Technical University of Athens, Greece, in 2005.

Designing coarse-grain reconfigurable architectures by ...

The coarse-grained reconfigurable architecture ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) and its compiler offer a tool flow to design sparsely interconnected 2D array processors with an arbitrary number of functional units, register files and interconnection topologies.

Architectural Exploration of the ADRES Coarse-Grained ...

Fine- and Coarse-Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine- (or FPGA) and Coarse-Grain Reconfigurable Architectures. Recently-developed

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integrated architecture design and software-supported design flow of FPGA and coarse-grain reconfigurable architecture are also described.

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